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EXAMINER	
KROFCHECK, MICHAEL C	
ART UNIT	**PAPER NUMBER**
2186	

DATE MAILED: 11/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/671,158	DELANEY ET AL.	
	Examiner	Art Unit	
	Michael Krofcheck	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☒ Claim(s) *10,18-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *9/25/2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/671,158 filed on September 25, 2003.

2. Claims 1 – 20 have been submitted for examination.

3. Claims 1 – 20 have been examined.

Drawings

4. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the I/O module in claims 4 and 5 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an

application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

5. The disclosure is objected to because of the following informalities:

a. In the bottom half of page 12 the host interface 204-2 is mistakenly referenced by reference number 20402.

Appropriate correction is required.

Claim Objections

6. Claims 10, 18 – 20 are objected to because of the following informalities:

a. In line 3 of claim 18, the word "first" is misspelled.

b. In line 2 of claims 10 and 20, the word, "an" should be replaced by, "a."

c. Claim 19 is objected to because of its dependency.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1, 2, 6, 7, and 11 – 17 are rejected under 35 U.S.C. 102(e) as being anticipated by Fujimoto et al., U.S. Patent No. 6,477,619.

9. With respect to claim 1, Fujimoto teaches of a storage system comprising: a first storage element (figs. 1, 7, 8, items 1-1-1 and 5), comprising a plurality of disk drives, each configured for storing data (figs. 1, 7, 8; item 5; column 6, lines 41 – 47); and

a first storage controller (figs. 1, 7, 8, item 1-1-1) communicatively coupled to a host computer system (item 1, 7, 8; item 50) and configured for processing I/O requests received from the host computer system (figs. 1, 7, 8; item 1-1-1; column 6, lines 41 – 47, column 7, 6 – 15; where the channel IF unit within the disk array control unit (first storage controller) interfaces with the host computers, and the channel IF unit controls access to the rest of the control unit),

wherein the first storage controller is adaptable to interface with a second storage controller added to the storage system within a second storage element (figs. 1; column 6, lines 41 – 55; where interconnections 210 and 220 connect the two disk array control units), and

wherein the first storage controller is further adaptable, when adapted to communicate with the second storage controller (figs. 1, 7, 8, item 1-1-2), to route the I/O requests to the second storage controller through a switching fabric (figs. 7, 8;

column 8, lines 1 – 17 and 32 –40; where the inter-unit paths 141 and 142 may be designed differently for Input and output or equally for bidirectional information transfer).

10. With respect to claim 2, Fujimoto teaches of all the limitations of the parent claim as discussed supra. Fujimoto also teaches of wherein the storage system is a RAID storage system (fig. 7; column 7, lines 33 – 34).

11. With respect to claim 6, Fujimoto teaches of a method of processing requests from a host computer system (figs. 1, 7, 8, item 50), comprising: transferring the requests from the host computer system to a first storage controller (figs. 1, 7, 8, item 1-1-1) of a first storage element (figs. 7, 8; column 9, lines 17 – 26, and 45 – 54; where the read out request is sent from the host computer to the disk array control unit 1-1-1. The disk array control unit 1-1-1 is associated with the hard disk drives 5 (1-1-1 and 5 comprise the first storage element), attached to itself); and

processing the requests to access physical storage locations within the first storage element (figs. 7, 8; column 9, lines 17 – 26, and 45 – 54; where the read out request is sent from the host computer to the disk array control unit 1-1-1. The microprocessor determines the location of the data requested and requests the microprocessor in the disk IF units of the corresponding hard drive to read out the data. If the data is located on a hard drive associated with the disk array control unit 1-1-1, then it is accessed by the microprocessor within the disk IF units of the disk array controller 1-1-1 to read out the requested data),

wherein transferring comprises forwarding a first portion of the requests from the first storage controller to a second storage controller (fig. 8, item 1-1-2) of a second

storage element (figs. 7, 8; column 9, lines 17 – 26, and 45 – 54; where the read out request is sent from the host computer to the disk array control unit 1-1-1. The microprocessor determines the location of the data requested and requests the microprocessor in the disk IF units of the corresponding hard drive to read out the data. For the part of the data located in a hard drive in the disk array control unit 1-1-2 (first portion of the requests), the microprocessor in the channel IF unit in the disk unit 1-1-1 must transfer that read request over the SM and CM paths (switching fabric) to a microprocessor in the disk array control unit 1-1-2. (items 1-1-2 and corresponding 5 comprise the second storage element)).

12. With respect to claim 7, Fujimoto teaches of all the limitations of the parent claim as discussed supra. Fujimoto also teaches of processing the first portion of the requests with the second storage controller to access physical storage locations within the second storage element (figs. 7, 8; column 9, lines 17 – 26, and 45 – 54; where the read out request is sent from the host computer to the disk array control unit 1-1-1. The microprocessor determines the location of the data requested and requests the microprocessor in the disk IF units of the corresponding hard drive to read out the data. For the part of the data located in a hard drive in the disk array control unit 1-1-2 (first portion of the requests), the microprocessor in the channel IF unit in the disk unit 1-1-1 must transfer that read request over the SM and CM paths (switching fabric) to the disk array control unit 1-1-2. It is then received by the microprocessor within the disk IF units of the disk array controller 1-1-2 associated with the desired hard drive which then reads out the data from the hard drive (processes the request)).

13. With respect to claim 8, Fujimoto teaches of all the limitations of the parent claim as discussed supra. Fujimoto also teaches of directly mapping a second portion of the requests to the physical storage locations within the first storage element (figs. 7, 8; column 9, lines 18 – 54; the read out request sent buy the host computer and received by the microprocessors in the channel IF unit of the disk array control unit 1-1-1. The microprocessors access the conversion table to locate the hard drives and addresses that correspond to the requested data. For the part of the requested data located in a hard drive or the cache memory controlled by disk array control unit 1-1-1 (second portion of the requests), then the address mapped for that location is therefore directed to the first storage element) and

directly mapping a third portion of the requests to the physical storage locations of the second storage element (figs. 7, 8; column 9, lines 18 – 54; the read out request sent buy the host computer and received by the microprocessors in the channel IF unit of the disk array control unit 1-1-1. The microprocessors access the conversion table to locate the hard drives and addresses that correspond to the requested data. For the part of the requested data located in a hard drive or the cache memory controlled by disk array control unit 1-1-2 (third portion of the requests), then the address mapped for that location is directed to the second storage element).

14. With respect to claim 11, Fujimoto teaches of a first storage controller (figs. 1, 7, 8, item 1-1-1) comprising: a host interface configured for communicatively coupling a host computer system (figs. 1, 7, 8, item 50) to a first storage element (figs. 7, 8; item 11; column 7, lines 6 – 34; column 8, lines 1 – 17; where the channel IF unit connects

the host computer to the hard disks via the SM and CM switches and the disk IF unit. Items 1-1-1 and corresponding item 5 comprise the first storage element);

a storage system interface configured for communicatively coupling the first storage element to a switching fabric (figs. 7, 8; column 7, lines 20 – 29; column 8, lines 1 – 17; where the disk array control unit (storage system interface) connects the hard drive to the SM and CM paths (switching fabric) through the disk IF unit and the SM and CM switches within); and

a processor configured for processing I/O requests received through the storage system interface and the host interface to access physical storage locations (figs. 7, 8; item 101; column 9, lines 17 – 26, and 45 – 54; where the microprocessor receives a read data request from the host computer and determines which hard disk stores the requested data),

wherein the storage system interface is further configured for transferring a portion of the I/O requests through the switching fabric to a second storage controller (figs. 7, 8; column 9, lines 17 – 26, and 45 – 54; where the microprocessor determines which hard drive the requested data is stored on and sends the read request to the microprocessor in the disk IF unit corresponding to where the data is stored. for the part of the data located in a hard drive in the disk array control unit 1-1-2, the microprocessor in the channel IF unit in the disk array control unit 1-1-1 must transfer that request over the SM and CM paths (switching fabric) to the disk array control unit 1-1-2 (second storage controller)).

15. With respect to claim 12, Fujimoto teaches of all the limitations of the parent claim as discussed supra. Fujimoto also teaches of wherein the first storage controller is adapted to route the portion of the I/O requests to a second storage element (figs. 7, 8; column 9, lines 17 – 26, and 45 – 54; where the microprocessor determines which hard drive the requested data is stored on and sends the read request to the microprocessor in the disk IF unit corresponding to where the data is stored. For the part of the data located in a hard drive in the disk array control unit 1-1-2, the microprocessor in the channel IF unit in the disk array control unit 1-1-1 must transfer that request to the microprocessor in the disk IF unit located in the disk array control unit 1-1-2) and

wherein the portion of the requests are processed by the second storage controller for accessing physical storage locations within the second storage element (figs. 7, 8; column 9, lines 45 – 54; where the microprocessor receiving the command in the disk IF unit of the disk array control unit 1-1-2 reads the data out of the hard drive).

16. With respect to claim 13, Fujimoto teaches of all the limitations of the parent claim as discussed supra. Fujimoto also teaches of a disk drive interface configured for communicatively coupling to a plurality of disk drives of the first storage element to access physical storage locations of the first storage element (figs. 1, 7, 8; item 12; column 7, lines 20 – 29).

17. With respect to claim 14, Fujimoto teaches of all the limitations of the parent claim as discussed supra. Fujimoto also teaches of the storage controller is a RAID storage controller (column 7, lines 33 – 34).

18. With respect to claim 15, Fujimoto teaches of all the limitations of the parent claim as discussed supra. Fujimoto also teaches of computer memory configured for storing software instructions, wherein the software instructions direct the processor to transfer the portion of the I/O requests through the switching fabric to the second storage controller of a second storage element (figs. 7, 8, item 13; column 9, lines 17 – 26, and 45 – 54; where the shared memory contains a conversion table which directs a search locating the hard drive that the requested data is stored in. When the data is located, the request is sent to the microprocessor in the disk IF unit corresponding to the hard drive storing the data. For the part of the data located in a hard drive in the disk array control unit 1-1-2, the microprocessor in the channel IF unit in the disk array control unit 1-1-1 must transfer that request over the SM and CM paths (switching fabric) to the disk array control unit 1-1-2).

19. With respect to claim 16, Fujimoto teaches of a method of storing data, comprising: configuring a first storage element (figs. 1, 7, 8, items 1-1-1 and 5) with a first storage controller capable (figs. 1, 7, 8, item 1-1-1) of interfacing with a host computer system (figs. 1, 7, 8, item 50) and a switching fabric (figs. 1, 7, 8; column 6, line 63 – column 7, line 35; column 8, lines 1 – 26; where the disk array controller 1-1-1 (first storage controller) communicates with the hard drives (first storage element) through the disk IF unit. The disk array controller is also connected to the host computer through the channel IF unit and is connected to the SM and CM paths (switching fabric) through the SM and CM switches); and at least one of:

transferring I/O requests from the host computer system to the first storage controller to access a plurality of physical storage locations within the first storage element (figs. 7, 8; column 9, lines 17 – 26, and 45 – 54; where the read out request is sent from the host computer to the disk array control unit 1-1-1. The microprocessor determines the location of the data requested and requests the microprocessor in the disk IF units of the corresponding hard drive to read out the data. If the data is located on a hard drive associated with the disk array control unit 1-1-1, then it is accessed by the microprocessor within the disk IF units of the disk array controller 1-1-1) and

transferring I/O requests from the host computer system through the switching fabric to a second storage controller (fig. 8, item 1-1-2) configured with a second storage element (figs. 7, 8; column 9, lines 17 – 26, and 45 – 54; where the read out request is sent from the host computer to the disk array control unit 1-1-1. The microprocessor determines the location of the data requested and requests the microprocessor in the disk IF units of the corresponding hard drive to read out the data. If the data is located in a hard drive in the disk array control unit 1-1-2, the microprocessor in the channel IF unit in the disk unit 1-1-1 must transfer that read request over the SM and CM paths (switching fabric) to the disk array control unit 1-1-2. It is then received by the microprocessor within the disk IF units of the disk array controller 1-1-2 associated with the desired hard drive. The second storage element comprises items 1-1-2 and corresponding item 5).

20. With respect to claim 17, Fujimoto teaches of all the limitations of the parent claim as discussed supra. Fujimoto also teaches of wherein transferring I/O requests

from the host computer system through the switching fabric to the second storage controller comprises processing the I/O requests with the second storage controller to access physical storage locations within the second storage element (figs. 7, 8; column 9, lines 17 – 26, and 45 – 54; where the read out request is sent from the host computer to the disk array control unit 1-1-1. The microprocessor determines the location of the data requested and requests the microprocessor in the disk IF units of the corresponding hard drive to read out the data. If the data is located in a hard drive in the disk array control unit 1-1-2, the microprocessor in the channel IF unit in the disk unit 1-1-1 must transfer that read request over the SM and CM paths (switching fabric) to the disk array control unit 1-1-2. It is then received by the microprocessor within the disk IF units of the disk array controller 1-1-2 associated with the desired hard drive which reads out the data (processes the request)).

21. With respect to claim 18, Fujimoto teaches of all the limitations of the parent claim as discussed supra. Fujimoto also teaches of directly mapping a first portion of the I/O requests transferred to the first storage controller to the physical storage locations within the first storage element (figs. 7, 8; column 9, lines 18 – 54; the read out request sent buy the host computer and received by the microprocessors in the channel IF unit of the disk array control unit 1-1-1. The microprocessors access the conversion table to locate the hard drives and addresses that correspond to the requested data. For the part of the requested data located in a hard drive or the cache memory controlled by disk array control unit 1-1-1 (first portion of the requests), then the address mapped for that location is directed to the first storage element) and

directly mapping a second portion of the I/O requests to the physical storage locations of the second storage element (figs. 7, 8; column 9, lines 18 – 54; the read out request sent buy the host computer and received by the microprocessors in the channel IF unit of the disk array control unit 1-1-1. The microprocessors access the conversion table to locate the hard drives and addresses that correspond to the requested data. For the part of the requested data located in a hard drive or the cache memory controlled by disk array control unit 1-1-2 (second portion of the requests), then the address mapped for that location is directed to the second storage element).

Claim Rejections - 35 USC § 103

22. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

23. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

24. Claims 3 – 5, 10, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujimoto and the applicant's prior art admission.

25. With respect to claim 3, Fujimoto teaches of all the limitations of the parent claim as discussed supra. Fujimoto also teaches of wherein the switching fabric is an SAN switching fabric communicatively coupled to the first and the second storage controllers and configured for routing the I/O requests between the host computer system and the first and the second storage controllers (figs. 1, 8; column 8, lines 32 – 40; column 2, lines 31 – 47; where the SM and CM paths (SAN switching fabric) between the disk array control units are made up of SM and CM switches (121 and 122). A SAN is described in Fujimoto to be met by an arrangement of a low level model of a conventional disk array controller connected to a plurality of identical controllers).

Fujimoto fails to explicitly teach of the SAN switching fabric comprising at least one of Fibre Channel and Infiniband. However, the applicant's admission of prior art teaches of the SAN switching fabric comprising at least one of Fibre Channel and Infiniband (spec. page 2, 2nd and 3rd paragraph).

Fujimoto and the applicant's prior art admission are analogous arts as they are both in the same field of endeavor, storage systems and controllers. It would have been obvious to one of ordinary skill in the art to implement the Fibre Channel and/or Infiniband standards in the switching paths between the disk array controllers in Fujimoto. The motivation for this would have been to allow for a greater distance between the storage systems and the host systems (applicant's prior art admission, spec. page 2, 2nd paragraph).

26. With respect to claim 4, Fujimoto and the applicant's prior art admission teach of all the limitations of the parent claims as discussed supra. Fujimoto also teaches of

wherein the storage system is adaptable to identify physical storage locations of both the first and the second storage elements using an I/O module added to the storage system when the first storage controller is adapted to communicate with the second storage controller (figs. 7, 8, item 13; column 9, lines 20 – 27; where the microprocessors access the shared memory units (I/O module) to determine the address and the hard disks that stores the requested data).

27. With respect to claim 5, Fujimoto and the applicant's prior art admission teach of all the limitations of the parent claims as discussed supra. Fujimoto also teaches of wherein the first storage controller comprises an N-chip configured for communicatively coupling to the SAN switching fabric to route a portion of the I/O requests from the host computer system through the SAN switching fabric to the second storage controller (figs. 1, 7, 8, items 110, 111, column 8, lines 1 – 17; column 9, lines 17 – 26, and 45 – 54; where the microprocessor in the channel IF unit of disk unit 1-1-1 determines which hard drive the requested data is stored on and sends the read request to the microprocessor in the disk IF unit corresponding to the hard drive that hold the data. For the part of the data located in a hard drive in the disk array control unit 1-1-2 (first portion of the requests), the microprocessor in the channel IF unit of disk unit 1-1-1 must transfer that request over the SM and CM paths (SAN switching fabric) to the disk array control unit 1-1-2. The SM and CM switches (N-chip) couple the controller to the SAN switching fabric),

wherein the N-chip is further configured for accessing data from the physical storage locations of both the first and the second storage elements to the I/O module

(figs. 1, 7, 8, items 110, 111, column 8, lines 1 – 17; where the SM and CM switches are connected to the two channel IF units, the two disk IF units, also the two shared memory units (I/O module) and cache memory units respectively, and are connected to the other disk array control unit via the SAN switching fabric).

28. With respect to claim 10, Fujimoto teaches of all the limitations of the parent claim as discussed supra. Fujimoto also teaches of wherein transferring the first portion of the requests comprises switching the first portion of the requests through an SAN switching fabric (figs. 7, 8; column 2, lines 31 – 47; column 9, lines 17 – 26, and 45 – 54; where the microprocessor in the channel IF unit of disk unit 1-1-1 determines which hard drive the requested data is stored on and sends the read request to the microprocessor in the disk IF unit corresponding to the hard drive that hold the data. For the part of the data located in a hard drive in the disk array control unit 1-1-2 (first portion of the requests), the microprocessor in the channel IF unit of disk unit 1-1-1 must transfer that request over the SM and CM paths (SAN switching fabric) to the disk array control unit 1-1-2. A SAN is described in Fujimoto to be met by an arrangement of a low level model of a conventional disk array controller connected to a plurality of identical controllers).

Fujimoto fails to explicitly teach of a SAN switching fabric selected from at least one of Fibre Channel and Infiniband. However, the applicant's prior art admission teaches of a SAN switching fabric selected from at least one of Fibre Channel and Infiniband (spec. page 2, 2nd and 3rd paragraph).

29. With respect to claim 20, Fujimoto teaches of all the limitations of the parent claim as discussed supra. Fujimoto also teaches of wherein transferring the I/O requests comprises switching the I/O requests through an SAN switching fabric (figs. 7, 8; column 2, lines 31 – 47; column 9, lines 17 – 26, and 45 – 54; where the microprocessor in the channel IF unit of disk unit 1-1-1 determines which hard drive the requested data is stored on and sends the read request to the microprocessor in the disk IF unit corresponding to the hard drive that hold the data. For the part of the data located in a hard drive in the disk array control unit 1-1-2, the microprocessor in the channel IF unit of disk unit 1-1-1 must transfer that request over the SM and CM paths (SAN switching fabric) to the disk array control unit 1-1-2. A SAN is described in Fujimoto to be met by an arrangement of a low level model of a conventional disk array controller connected to a plurality of identical controllers).

Fujimoto fails to explicitly teach of a SAN switching fabric selected from at least one of Fibre Channel and Infiniband. However, the applicant's prior art admission teaches of a SAN switching fabric selected from at least one of Fibre Channel and Infiniband (spec. page 2, 2nd and 3rd paragraph).

30. Claims 9 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujimoto and Reuter et al., U.S. Patent Application Publication No. 2002/0019922 (hereinafter Reuter).

31. With respect to claim 9, Fujimoto teaches of all the limitations of the parent claim as discussed supra. Fujimoto teaches of addressing the storage locations of the first and second storage elements (as previously cited).

Fujimoto fails to specifically teach of wherein mapping comprises translating virtual storage addresses into physical addresses to access the physical storage locations.

However, Reuter teaches of wherein mapping comprises translating virtual storage addresses into physical addresses to access the physical storage locations (fig. 2; paragraphs 0012, 0013, 0017 – 0019; where the host issues an I/O requests and mapping agents perform the necessary mapping from the mapping table and issue the resulting I/O requests to the physical storage. Each mapping table entry represents a group of virtual disk blocks that map to blocks on one of the physical storage devices).

Fujimoto and Reuter are analogous arts as they are both in the same field of endeavor, data storage systems. It would have been obvious to one of ordinary skill in the art having the teachings of Fujimoto and Reuter at the time of the invention to make the conversion table in the shared memory of Fujimoto a table that maps a virtual disk location to a physical location as the mapping table in Reuter. The motivation for this would have been to allow new storage management value to be introduced including the ability to migrate data among physical storage devices without effecting the host view of the data (Reuter, paragraphs 0003 and 0004).

32. With respect to claim 19, Fujimoto teaches of all the limitations of the parent claim as discussed supra. Fujimoto teaches of addressing the storage locations of the first and second storage elements (as previously cited).

Fujimoto fails to specifically teach of wherein mapping comprises translating virtual storage addresses into physical addresses to access the physical storage locations.

However, Reuter teaches of wherein mapping comprises translating virtual storage addresses into physical addresses to access the physical storage locations (fig. 2; paragraphs 0012, 0013, 0017 – 0019; where the host issues an I/O requests and mapping agents perform the necessary mapping from the mapping table and issue the resulting I/O requests to the physical storage. Each mapping table entry represents a group of virtual disk blocks that map to blocks on one of the physical storage devices).

Conclusion

33. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

34. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Krofcheck whose telephone number is 571-272-8193. The examiner can normally be reached on Monday - Friday.

35. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

36. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Michael Krofcheck

MATTHEW D. ANDERSON
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